<u>What is Claimed Is:</u>

1.   A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining sub-module of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system

synthesizing gate-level designs of the sub-module based on the determined time budgets for the individual sub-modules;

integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.

2.   The method of claim 1, further comprising generating gate-level netlists for the gate-level designs of each of the sub-modules.

3.   The method of claim 2, wherein the step of integrating the gate-level designs includes integrating the gate-level netlists of the sub-modules.

4.   The method of claim 3, further comprising testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules prior to integrating the gate-level designs to form the top-level design.

5.   The method of claim 4, wherein testing the gate-level designs include performing static timing analysis on the individual sub-modules for conformance with timing requirements for the individual sub-blocks.

6.   The method of claim 5, wherein the gate-level netlists are generated for the sub-modules only if the timing requirements for the individual sub-modules are met.

7.   The method of claim 6, wherein the step of synthesizing is re-performed and the gate-level designs are re-tested in an iterative manner for verifying conformance of the gate-level designs with the timing requirements of the individual sub-modules.

8.   The method of claim 7, wherein the step of synthesizing gate-level designs is further based on wire loads and input/output loads/drivers.

9.   The method of claim 8, wherein the step of verifying conformance of the gate-level designs includes performing dynamic simulations on the gate-level designs.